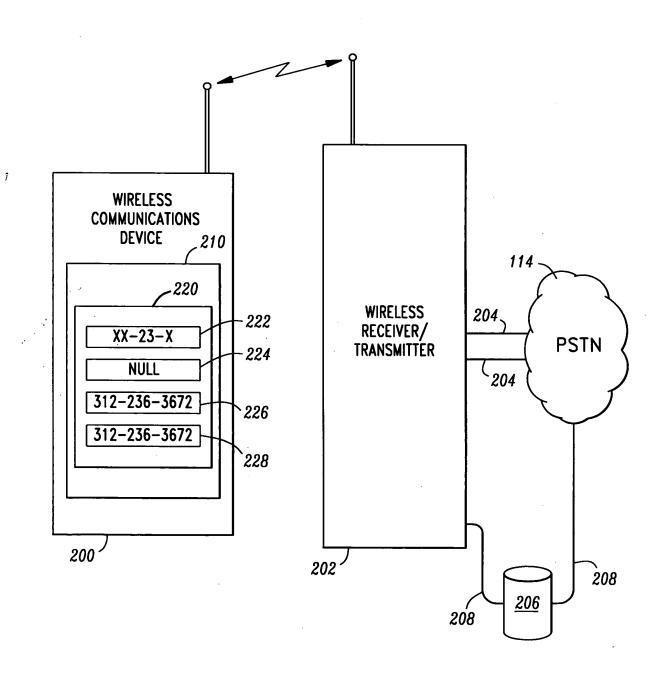
FIG. 1 100 _104 **MEMORY** 120a 120b 120x 122a 122b XXX-X-01 XXX-X-02 122 X 124b 124a 312-236-3672 NULL 124X 126a 312-236-3672 312-236-3672 126 X 128a 126b 312-236-3672 312-236-3672 128x 128b -102 -108 **PROCESSOR SWITCHING** 106-**INTERFACE** LINE INTERFACE 01 02 112 112-110c 110x 110a -114 110b 116 **PSTN** 119 118

i)

FIG. 2



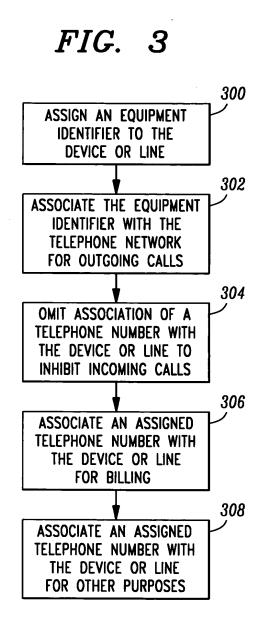
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FIG. 4



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